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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,683	09/23/2003	Andre Schaefer	30169/30001	1058

4743 7590 09/27/2005

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EXAMINER

TON, MY TRANG

ART UNIT PAPER NUMBER

2816

DATE MAILED: 09/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/668,683

Applicant(s)

SCHAEFER ET AL.

Examiner

My-Trang N. Ton

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 4-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 4-9 is/are allowed.
- 6) ☒ Claim(s) 1 and 10-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.



MY-TRANG NUTON
PRIMARY EXAMINER

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 10-12 remain rejected under 35 U.S.C. 102(e) as being anticipated by Jong et al (U. S Patent No. 6,737,892).

As recited in previous Office action, Jong et al disclose in Fig. 3 a system for detecting a valid clock signal at a clock receiver including:

Regarding claim 1: a circuit device (101, Fig. 1) comprising at least a first connection (CK+122) and a second connection (CK+123), whereby {a single clock pulse can be applied to the first connection or a differential clock pulse (CK+122, CK-123) can be applied to the first and second connection (CK+122, CK-123) and a detection facility (120, Fig. 1) to detect whether there is a differential clock pulse (CK+122, CK+123) present at the first and second connection (CK+122, CK-123, see col. 4, lines 16-21, lines 58-63, col. 5, lines 12-48 discloses detecting a valid clock signal) {or a single clock pulse present at the first connection} (It is noted that: due to “or” condition, the claims only required to met one condition, thus the phrase inside { } is not considered), the detection facility (120, Fig. 1) having a first state (High state), if a differential clock pulse (CK+122, CK-123) is present at the first and second connections

Art Unit: 2816

(CK+122, CK-123) in which a first output signal is provided, and a second state, {if a single clock pulse is present at the first connection, in which a second output signal different than the first output signal is provided} (it should be noted that in view of the term "or" recited above, the claim is not seen to require that the circuit met the second "if" function).

Claim 10 is similarly rejected as claim 2:

at least a first connection (connected to CK-123), to which a clock pulse (CK-123) can be applied, and a second connection (connected to CK+122), to which a clock pulse (CK+122) can be applied; and

a detection (120, Fig. 1) facility which in determining {whether a clock pulse is present at the second connection, determines} whether there are differential clock pulses (CK+122, CK-123) present at the connection, {or whether there is a single clock pulse present at the first connection, but not at the second connection}, (It is noted that: due to "or" condition, the claims only required to met one condition, thus the phrase inside { } is not considered),

the detection facility (120, Fig. 1) having a first state (High state), if differential clock pulses (CK+122, CK-123) are present at the connections (connected to CK-123 and CK+122), in which a first output signal is provided, and a second state, {if a single clock pulse is present at the first connection, in which a second output signal different than the first output signal is provided} (it should be noted that in view of the term "or" recited above, the claim is not seen to require that the circuit met the second "if" function) .

Art Unit: 2816

The limitation recited in claims 11-12 are seen to define intended use. The clock detection circuit of Jong is capable of using for DDR memory component and the memory component is a DRAM as recited. In re Tuominen, 213 USPQ 89 (CCPA 1982) & In re Pearson, 494 F.2d 1399, 181 USPQ 641 (CCPA 1974).

Claims 1 and 10-12 also remain rejected under 35 U.S.C. 102(e) as being anticipated by Hattori (U. S Patent No. 6,791,369).

Hattori disclose in Figs. 6-8 a differential-clock detector circuit including:

Regarding claim 1: a circuit device (40) comprising at least a first connection (CK+) and a second connection (CK-), whereby {a single clock pulse can be applied to the first connection or a differential clock pulse (CK+, CK-) can be applied to the first and second connection (CK+, CK-) and a detection facility (40) to detect whether there is a differential clock pulse (CK+, CK-) present at the first and second connection (CK+, CK-, presence or absence of the differential clock is detected, see col. 5, line 15- col. 6, line 39) or a single clock pulse present at the first connection}. (It is noted that: due to "or" condition, the claims only required to met one condition, thus the phrase inside { } is not considered), the detection facility (40) having a first state (High state), if a differential clock pulse (CK+, CK-) is present at the first and second connections (CK+, CK-) in which a first output signal is provided, and a second state, {if a single clock pulse is present at the first connection, in which a second output signal different than the first output signal is provided} (it should be noted that in view of the term "or" recited above, the claim is not seen to require that the circuit met the second "if" function).

Claim 10 is similarly rejected as claim 2:

at least a first connection (connected to CK-), to which a clock pulse (CK-) can be applied, and a second connection (connected to CK+), to which a clock pulse (CK+) can be applied; and

a detection (40) facility which in determining {whether a clock pulse is present at the second connection, determines} whether there are differential clock pulses (CK+, CK-) present at the connection, {or} whether there is a single clock pulse present at the first connection, but not at the second connection}, (It is noted that: due to "or" condition, the claims only required to met one condition, thus the phrase inside { } is not considered),

the detection facility (40) having a first state (High state), if differential clock pulses (CK+, CK-) are present at the connections (connected to CK- and CK+), in which a first output signal is provided, and a second state, {if a single clock pulse is present at the first connection, in which a second output signal different than the first output signal is provided} (it should be noted that in view of the term "or" recited above, the claim is not seen to require that the circuit met the second "if" function).

The limitation recited in claims 11-12 are seen to define intended use. The clock presence detector circuit of Hattori is capable of using for DDR memory component and memory component is a DRAM as recited. In re Tuominen, 213 USPQ 89 (CCPA 1982) & In re Pearson, 494 F.2d 1399, 181 USPQ 641 (CCPA 1974).

Allowable Subject Matter

Claims 4-9 are allowable over the prior art of record.

Art Unit: 2816

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



My-Trang N. Ton
Primary Examiner
Art Unit 2816

September 26, 2005